CLAIMS

WHAT IS CLAIMED:

1. A method of removing sidewall spacers of a semiconductor structure, the method comprising:

providing a substrate having partially formed thereon semiconductor devices, the devices comprising first and second sidewall spacers with first and second etch rates with respect to a specific etchant, whereby said first etch rate is lower than said second etch rate;

implanting ions into said first sidewall spacers to adapt said first etch rate to said second etch rate; and

removing said first and second sidewall spacers with the specific etchant, whereby a selectivity in removing said first and second sidewall spacers is increased by the implanting of said ions.

2. The method of claim 1, wherein said partially formed semiconductor devices are partially formed N-type and P-type field effect transistors.

3. The method of claim 1, wherein said semiconductor structure is a CMOS structure.

4. The method of claim 1, wherein a mask covering at least said second sidewall spacers is employed to implant said ions into said first sidewall spacers.

5. The method of claim 4, wherein said mask is formed by photolithography.

6. The method of claim 4, wherein said mask is one of a photoresist mask and a hard mask.

7. The method of claim 6, wherein said photoresist mask has a thickness of approximately 100-2000 nm

8. The method of claim 1, wherein said ions are substantially inert ions.

9. The method of claim 1, wherein said ions are at least one of argon ions, xenon ions, germanium ions and silicon ions.

10. The method of claim 1, wherein the ion implant dose is in the range of approximately 1×10^{13} to 1×10^{15} ions/cm^2.

11. The method of claim 1, wherein the ion energy is in the range of approximately 10-80 keV.

12. The method of claim 1, wherein a tilt angle between a surface of said substrate and a direction of incidence of said ions is in the range of approximately 10-70 degrees.

13. The method of claim 1, wherein the material of said sidewall spacers comprises an inorganic material.

14. The method of claim 1, wherein the material of said sidewall spacers comprises a low-k material.

15. The method of claim 1, wherein the material of said sidewall spacers is silicon nitride.

16. The method of claim 1, wherein, prior to the step of implanting ions into said sidewall spacers, dopants are implanted into said sidewall spacers during the formation of a source and a drain region in said partially formed semiconductor device.

17. The method of claim 16, wherein said dopants are at least one of boron, arsenic and phosphorous.

18. The method of claim 1, wherein said partially formed semiconductor device comprises a gate feature and the measure of said gate feature in one direction is approximately 100 nm or less.

19. A method of removing sidewall spacers of a semiconductor structure, the method comprising:

providing a substrate having partially formed thereon semiconductor devices, the devices comprising first and second sidewall spacers with first and second etch rates to a specific etchant, whereby said first etch rate is lower than said second etch rate;

implanting ions into said first and second sidewall spacers to increase said first and second etch rates; and

removing said first and second sidewall spacers with the specific etchant, whereby a selectivity in removing said first and second sidewall spacers is increased by the implanting of ions.

20. The method of claim 19, wherein said partially formed semiconductor devices are partially formed N-type and P-type field effect transistors.

21. The method of claim 19, wherein said semiconductor structure is a CMOS structure.

22. The method of claim 19, wherein said ions are substantially inert ions.

23. The method of claim 19, wherein said ions are at least one of argon ions, xenon ions, germanium ions and silicon ions.

24. The method of claim 19, wherein the ion dose is in the range of approximately 1×10^{14} to 1×10^{15} ions/cm^2.

25. The method of claim 19, wherein the ion energy is in the range of approximately 10-80 keV.

26. The method of claim 19, wherein a tilt angle between a surface of said substrate and a direction of incidence of said ions is in the range of approximately 10-85 degrees.

27. The method of claim 19, wherein the material of said sidewall spacers comprises an inorganic material.

28. The method of claim 19, wherein the material of said sidewall spacers comprises a low-k material.

29. The method of claim 19, wherein the material of said sidewall spacers comprises silicon nitride.

30. The method of claim 19, wherein, prior to said implanting of ions, dopants are implanted into said sidewall spacers during the formation of a source and a drain region.

31. The method of claim 30, wherein said dopants are at least one of boron, arsenic and phosphorous.

32. The method of claim 19, wherein said partially formed semiconductor devices comprise a gate feature and a dimension of said gate feature in at least one direction is 100 nm or less.